

Exercises in System Level Programming (SLP) – Summer Term 2025

Exercise 6

Maxim Ritter von Onciul
Eva Dengler

Lehrstuhl für Informatik 4
Friedrich-Alexander-Universität Erlangen-Nürnberg



Lehrstuhl für Informatik 4
Systemsoftware



Friedrich-Alexander-Universität
Faculty of Engineering

Presentation Assignment 3

Interrupts



- Procedure of an interrupt (see 18-7):
 0. Hardware sets required flag
 1. If interrupts are enabled and the interrupt is not masked, the interrupt controller interrupts the current execution
 2. Further interrupts are disabled
 3. Current program position is saved
 4. Address of the handler is read from the interrupt vector table and is then jumped to
 5. The interrupt handler is executed
 6. At the end of the interrupt handler, the instruction “return from interrupt” returns to the interrupted program and then re-enables the interrupts



- For every interrupt, one bit for storing its state is available
- May lead to lost interrupts: An interrupt occurs during...
 - the execution of an interrupt handler (interrupts too fast)
 - disabled interrupts section (for synchronization of critical sections)
- This problem cannot be prevented in general
- ~> Risk minimization: Interrupt handler shall be as short as possible
 - Avoid any kind of loops and function calls
 - Do not use any blocking function (ADC/serial interface!)



- Timer
- Serial interface
- ADC (analog digital converter)
- External interrupts by level changes at certain I/O pins
 - Choice of level- or edge-triggered
 - Depend on the interrupt source
 - ⇒ ATmega328PB: 2 sources at the pins PD2 (INT0) and PD3 (INT1)
 - ⇒ BUTTON0 at PD2
 - ⇒ BUTTON1 at PD3
- More details in the ATmega328PB data sheet



- Interrupts can be enabled and disabled by special machine instructions
- The library `avr-libc` provides useful macros:
`#include <avr/interrupt.h>`
 - `sei()` (set interrupt flag): enables interrupts (delayed by one instruction)
 - `cli()` (clear interrupt flag): disables all interrupts (immediately)
- Upon entering an interrupt handler, all interrupts are disabled automatically and re-enabled again as soon as the handler is exited
- `sei()` should never be called from inside an interrupt handler
 - Potentially infinitely nested interrupt handlers
 - Possibility of a stack overflow
- At the start of the μC , interrupts are disabled by default



- Interrupt sense control (ISC) bits of the ATmega328PB are located at the external interrupt control register A (EICRA)
- Position of the ISC-bits inside the register defined by macros

Interrupt INT0		Interrupt on	Interrupt INT1	
ISC01	ISC00		ISC11	ISC10
0	0	low level	0	0
0	1	either edge	0	1
1	0	falling edge	1	0
1	1	rising edge	1	1

- Example: Configuring INT1 of the ATmega328PB for a falling edge

```
01 /* the ISC-bits are located in the EICRA */
02 EICRA &= ~(1 << ISC10); // deleting ISC10
03 EICRA |= (1 << ISC11); // setting ISC11
```



- Single interrupts can be enabled (= unmasked) individually
 - ATmega328PB: External interrupt mask register (EIMSK)
- The bit positions inside of the register are defined by macros `INTn`
- A set bit enables the corresponding interrupt
- Example: Enabling the external interrupt `INT1`

```
01 EIMSK |= (1 << INT1); // Unmask the external interrupt INT1
```



- Registering an interrupt handler is implemented by the C library
- Macro ISR (interrupt service routine) used for defining a handler function (`#include <avr/interrupt.h>`)
- Parameter: Desired vector
 - Available vectors: Refer to avr-libc documentation for `avr/interrupt.h`
 - Example: `INT1_vect` for external interrupt `INT1`
- Example: Implement handler for `INT1`

```
01 #include <avr/interrupt.h>
02
03 static volatile uint16_t counter = 0;
04
05 ISR(INT1_vect) {
06     counter++;
07 }
```

Synchronization



- When an interrupt occurs, `event = 1` is set
- Active waiting loop waits until `event != 0`
- Compiler detects that `event` is not changed within the loop
 - ⇒ the value of `event` is only loaded once from memory into a processor register
 - ⇒ endless loop
- `volatile` enforces that the variable is loaded from memory before every access

```
01 static uint8_t event = 0;
02 ISR(INT0_vect) {
03     event = 1;
04 }
05
06 void main(void) {
07     while(1) {
08         while(event == 0) { /* wait for event */ }
09         // handle event [...]
10     }
11 }
```



- Missing `volatile` can lead to unexpected program execution
 - Unnecessary use of `volatile` prevents certain compiler optimizations
 - Correct use of `volatile` is task of the programmer!
- ~> Use `volatile` as rarely as possible but as often as required



- Counting button presses that have to be processed
 - Incremented in the interrupt handler
 - Decrement in the main program to start the processing

```
01 static volatile uint8_t counter = 0;
02 ISR(INT0_vect) {
03     counter++;
04 }
05
06 void main(void) {
07     while(1) {
08         if(counter > 0) {
09
10             counter--;
11
12             // handle pressed button
13             // [...]
14         }
15     }
16 }
```



Main program

```
01 ; C instruction: counter--;  
02 lds r24, counter  
03 dec r24  
04 sts counter, r24
```

```
01 ; C instruction: counter--;  
02 lds r24, counter  
03 dec r24  
04 sts counter, r24
```

```
01 ; C instruction: counter--;  
02 lds r24, counter  
03 dec r24  
04 sts counter, r24
```

```
01 ; C instruction: counter--;  
02 lds r24, counter  
03 dec r24  
04 sts counter, r24
```

Interrupt handler

```
05 ; C instruction: counter++  
06 lds r25, counter  
07 inc r25  
08 sts counter, r25
```

```
05 ; C instruction: counter++  
06 lds r25, counter  
07 inc r25  
08 sts counter, r25
```

```
05 ; C instruction: counter++  
06 lds r25, counter  
07 inc r25  
08 sts counter, r25
```

```
05 ; C instruction: counter++  
06 lds r25, counter  
07 inc r25  
08 sts counter, r25
```



- Concurrent use of 16 bit values (read write)
 - Incrementing in the interrupt handler
 - Reading in the main program

```
01 static volatile uint16_t counter = 0;
02 ISR(INT0_vect) {
03     counter++;
04 }
05
06 void main(void) {
07     if(counter > 300) {
08         sb_led_on(YELLOW0);
09     } else {
10         sb_led_off(YELLOW0);
11     }
12
13     // [...]
14 }
```



Main program

```
01 ; C instruction: if(counter>300)
02 lds r22, counter
03 lds r23, counter+1
04 cpi r22, 0x2D
05 sbci r23, 0x01
```

```
01 ; C instruction: if(counter>300)
02 lds r22, counter
03 lds r23, counter+1
04 cpi r22, 0x2D
05 sbci r23, 0x01
```

```
01 ; C instruction: if(counter>300)
02 lds r22, counter
03 lds r23, counter+1
04 cpi r22, 0x2D
05 sbci r23, 0x01
```

```
01 ; C instruction: if(counter>300)
02 lds r22, counter
```

Interrupt handler

```
07 ; C instruction: counter++;
08 lds r24, counter
09 lds r25, counter+1
10 adiw r24,1
11 sts counter+1, r25
12 sts counter, r24
```

```
07 ; C instruction: counter++;
08 lds r24, counter
09 lds r25, counter+1
10 adiw r24,1
11 sts counter+1, r25
12 sts counter, r24
```

```
07 ; C instruction: counter++;
08 lds r24, counter
09 lds r25, counter+1
10 adiw r24,1
11 sts counter+1, r25
12 sts counter, r24
```



- Many more concurrency problems are possible
 - Non-atomic modification of shared data
 - Analysis of the problem by the application programmer
 - Choice of suitable synchronization primitives
 - Solution here: Mutual exclusion by disabling interrupts
 - Disable all interrupts: `cli()` and `sei()`
 - Disabling single interrupts (EIMSK-register)
 - Problem: Interrupts can be lost during a critical section
- ⇒ Critical sections have to be as short as possible



■ How can a lost update be prevented?

```
01 static volatile uint8_t counter = 0;
02 ISR(INT0_vect) {
03     counter++;
04 }
05
06 void main(void) {
07     while(1) {
08         if(counter > 0) {
09
10             counter--;
11
12             // handle pressed button
13             // [...]
14         }
15     }
16 }
```

```
01 static volatile uint8_t counter = 0;
02 ISR(INT0_vect) {
03     counter++;
```



- How can a read-write anomaly be prevented?

```
01 static volatile uint16_t counter = 0;
02 ISR(INT0_vect) {
03     counter++;
04 }
05
06 void main(void) {
07
08
09
10     if(counter > 300) {
11
12         sb_led_on(YELLOW0);
13     } else {
14
15         sb_led_off(YELLOW0);
16     }
17
18     // [...]
19 }
```

Power-Saving Modes



- AVR-based devices are often powered by batteries (e.g. remotes)
- Saving energy can drastically extend the life span
- AVR processors support multiple power-saving modes
 - Deactivating functional units
 - Different “depths” of sleep
 - Only active functional units can wake up the CPU
- Default mode: Idle
 - CPU clock is stopped
 - No more memory accesses
 - Hardware (timer, external interrupts, ADC, etc.) are still active
- Documentation in ATmega328PB data sheet



- Support from the avr-libc: (`#include <avr/sleep.h>`)
 - `sleep_enable()` - enables the sleep mode
 - `sleep_cpu()` - enters the sleep mode
 - `sleep_disable()` - disables the sleep mode
 - `set_sleep_mode(uint8_t mode)` - configures the used mode
- Documentation of `avr/sleep.h` in avr-libc documentation

```
01 #include <avr/sleep.h>
02
03 set_sleep_mode(SLEEP_MODE_IDLE); // use idle mode
04 sleep_enable();    // activate sleep mode
05 sleep_cpu();       // enter sleep mode
06 sleep_disable();   // recommended: deactivate sleep mode
    ↪ afterwards
```

- Sleeping beauty (german: *Dornröschenschlaf*)
 - ⇒ **Problem:** There is exactly one interrupt
 - ⇒ **Solution:** Disable interrupts during the critical area

Main program

```
01 sleep_enable();
02 event = 0;
03
04
05 while(!event) {
06     sleep_cpu();
07 }
08
09
10
11
12 sleep_disable();
```

```
01 sleep_enable();
02 event = 0;
03
```

Interrupt handler

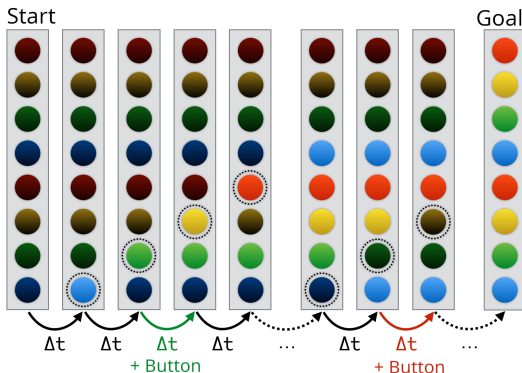
```
01 ISR(TIMER1_COMPA_vect) {
02     event = 1;
03 }
```

```
01 ISR(TIMER1_COMPA_vect) {
02     event = 1;
03 }
```

```
01 ISR(TIMER1_COMPA_vect) {
02     event = 1;
03 }
```

Assignment: Dexterity Game

- Game cursor moves over the LED strip and inverts (toggles) the state of the LED
- LED state is retained if the button is pressed
- Goal: Switch on all LEDs





- After each level, a winning sequence is displayed via the LEDs

```
01 void main(void) {  
02     // Initialisation  
03     // [...]  
04  
05     while(1) {  
06         // starting level  
07         // [...]  
08  
09         // show win sequence  
10         // [...]  
11  
12         // update level  
13         // [...]  
14     }  
15 }
```



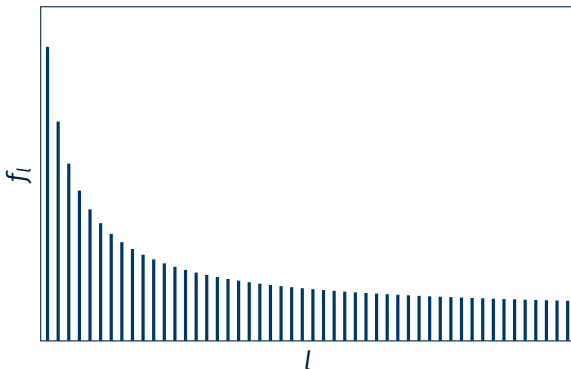
■ Goals:

- Edge detection in hardware
- Handle events using interrupts
- **No** use of the `libspicboard`

■ Details:

- `BUTTON0` is wired to `PD2`
- Configure `PD2` as input (with activated pull-up resistor)
- `PD2` is input of `INT0`
- Which level/edge has to be configured for the interrupt?
- How does a minimal interrupt handler for this assignment look like?

- Speed of the game determines its difficulty
 - ⇒ Passive waiting with the timer module of the libspicboard
- Difficulty increases with each level l
- Speed converges to a maximum
 - ⇒ Series of waiting times: $f_l = \frac{a}{l} + b$ (a and b are constants)





- Counting activations of BUTTON0 (PD2)
- Detect activation with the help of interrupts
- Output the current counter value using the 7-segment display
- Enter a CPU sleeping state whenever the **value is even**
- “Standby” LED switched on during the sleep mode (BLUE0)
- Hints:
 - Detection of the activation **without** the libspicboard
 - PD2/BUTTON0 is the input of INT0
 - Interrupt on a falling edge:
 - `EICRA(ISC00) = 0`
 - `EICRA(ISC01) = 1`
 - 7-segment display needs regular interrupts to display values